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Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of

Inventor(s): Joseph B. Bernstein and Zhihui Duan

Title: LASER-INDUCED CUTTING OF METAL INTERCONNECT

- ☒ Specification, Claims, Abstract of the Disclosure
- ☒ 7 sheets of ~~XXXXXX~~ formal/informal drawings. (Figs. 1-14)
- ☒ An assignment of the invention to Massachusetts Institute of Technology
(2 Assignment Forms) University of Maryland
- ☐ A verified statement to establish small entity status under 37 C.F.R. 1.9 and 37 C.F.R. 1.27.
- ☒ Executed ~~XXXXXX~~ Combined Declaration/Power of Attorney. (2 Declarations)
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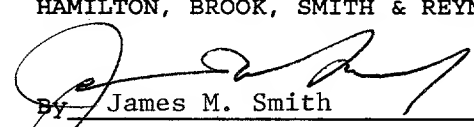
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Respectfully submitted,

HAMILTON, BROOK, SMITH & REYNOLDS

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Dated: 4/3/97
APPATENT.LTR-REV. 10/01/96

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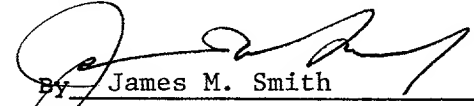
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-1-

LASER-INDUCED CUTTING OF METAL INTERCONNECT

BACKGROUND OF THE INVENTION

The use of lasers to cut integrated circuits is well-known in the art. In existing methods, a laser is directed
5 onto a cut-link segment of the circuit. The laser supplies sufficient heat to vaporize the cut-link, thereby severing the cut-link. In many cases such as in a typical microchip, the circuit is coated with a passivation layer to protect the circuit from oxidation. To allow the cut-
10 link to vaporize, the passivation layer is usually etched away from the site above the cut-link to expose the cut-link to the atmosphere in advance of cutting.

Lasers are used to cut circuits for a variety of purposes including the avoidance of defects, the
15 replacement of defective circuits with redundant circuits, and the programming of circuits. The practices used to achieve each of these objectives are described, below.

Lasers have been used to avoid defects by circumventing a short through laser-induced cuts. This
20 practice is described in U.S. Patent No. 4,259,367, issued to Doherty, Jr. The circuit is repaired by using a laser to cut the lines connected to the short to thereby isolate the short. Patch lines may then be used to reestablish severed connections.

25 The use of redundant circuitry has become an industry standard for memory chip fabrication. Redundant circuitry in a chip is typically supplied in the form of identical segments of circuitry occupying remote areas on the chip. If a segment is flawed, that segment is disconnected and
30 replaced by activating its redundant counterpart elsewhere on the chip.

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Finally, circuits may be programmed by cutting lines from a generic, repeating pattern to disconnect unwanted or unnecessary segments and thereby produce the desired pattern through a process of reduction. Circuitry produced
5 by this method may extend across a plurality of levels as well. One example of multi-level circuit design by laser-induced cutting is disclosed in U.S. Patent No. 4,720,470, issued to Johnson.

Typically, the cut-link has taken one of two forms.
10 First, the cut-link is often an undistinguished segment of a line in the circuit, where the width of the cut-link is equal to the width of the lines to which it is conductively coupled. A cut-link exhibiting these characteristics is illustrated in Figure 1 and disclosed, for example, in the
15 following U.S. patents: No. 4,853,758, issued to Fischer, and No. 5,589,706, issued to Mitwalsky et al. The second common form is that of a "dog bone," which is illustrated in Figure 2. This design is disclosed, for example, in the following U.S. patents: No. 4,748,491, issued to Takagi,
20 and No. 5,374,590, issued to Batdorf et al. In this design, the cut-link 20 is narrower than the lines 21, 22 to which it is connected.

DISCLOSURE OF THE INVENTION

Whereas the design of earlier cut-links mirrors the
25 narrowed "dog-bone" of conventional fuse design, a preferred embodiment of this invention rejects this model and, instead, widens the segment where the circuit is to be severed. Where circuitry is cut by a laser, the high resistance of a fuse is not required to produce the needed
30 influx of thermal energy. In this context, the thermal energy needed to melt the conductive material is supplied by an external source, i.e., the laser. As the present inventors have recognized, the use of the laser frees the designer from the necessity of using a high resistance

segment to generate the heat necessary to cut the circuit. Although intuition might further suggest that a fuse-shaped cut-link of thin width could be severed with greater precision and efficiency than an otherwise comparable cut-link of greater width, the present inventors have
5 recognized that this notion is generally false.

To the contrary, an electrical interconnect which may be cut with greater success and with improved efficiency includes a cut-link pad in which the thermal resistance per
10 unit length is lower, rather than higher, than the connected lines. In a preferred embodiment, the thermal resistance is lowered by adopting a form that is the inverse of the traditional "dog bone" design. The form of this new design is such that the width of the cut-link pad
15 is substantially greater than the width of the lines.

The electrical interconnect of this invention includes an insulating substrate upon which a pair of electrically-conductive lines are bonded to a cut-link pad, wherein the cut-link pad has substantially less thermal resistance per
20 unit length, *i.e.*, along the axis of the lines, than each of the lines to which it is bonded. The cut-link pad may lie in the same plane as the lines, or the pad may lie on a plane which is merely intersected by the lines, as in a via structure where the lines, or vias, extend from the
25 underside of the pad into the substrate to a lower level of circuitry. Alternatively, the cut-link pad may be bonded both to a line on the same plane as the pad and also to a via extending from the pad deeper into the substrate.

In a preferred embodiment of the electrical
30 interconnect, the thermal resistance of the pad is decreased, relative to the lines, by increasing the width of the pad such that the pad's width is greater than that of the lines to which it is connected. Benefit is provided in an interconnect where the cut-link pad is just 10
35 percent greater than the width of each of the lines.

the following reasons. First, the structures of the present invention retain thermal energy at the site of the cut-link more effectively than the cut-links of the prior art by restricting dissipative heat transfer from the cut-link into the connected lines. Second, the shapes of preferred structures produce increased stress at the perimeter of the cut-link pad, thereby generating a more forceful fracture of the surrounding material. Third, the shapes of preferred structures create stress concentration points that will produce fractures radiating outwardly from the site of the cut-link pad, thereby improving the likelihood that the fracture will be clean, *i.e.*, will not create inter-linked fracture passages through which escaping metal may form a "short" defeating the attempt to cleanly sever the circuit. Fourth, where the cut-link pad more closely approximates the size and shape of the laser beam, the cut-link absorbs a greater portion of the laser's energy, thereby producing a more efficient transfer of energy and a reduced danger of damaging the surrounding material. Fifth, where a passivative coating comprised of a brittle material is used, the fracture is biased toward the passivative coating, and, hence, toward the surface of a chip for efficient removal of the passivative coating and non-damaging expulsion of the metal comprising the cut-link pad. Sixth, by trapping the heat within the confines of the cut-link pad and limiting its escape through the connected lines, the site at which the cut develops is confined within this narrow region and damage to other parts of the circuit is minimized. Each of these phenomena will be discussed in greater detail and with greater clarity in the context of describing the structure and methods of several preferred embodiments of this invention.

Figure 8 is a cross-sectional illustration of an electrical interconnect, from a perspective normal to the plane of the substrate, where the width of each of the lines is equal to the width of the cut-link pad, except in
5 the vicinity of the juncture between the line and the pad, where the width of the line narrows.

Figure 9 is a cross-sectional illustration similar to Figure 8, except that the cut-link pad is in the form of a hexagon, rather than a square.

10 Figure 10 is a side-view, through the substrate, of a multi-level via structure from a perspective within the plane of the substrate.

Figure 11 is a view of the multi-level circuit of Figure 10 from underneath the via structure.

15 Figure 12 is a chart illustrating the approximate shape of a cumulative probability function measuring the likelihood that a circuit will be cut over a range of energy levels.

Figure 13 is a chart illustrating the approximate
20 shape of a cumulative probability function measuring the likelihood that the integrated circuit will be damaged over the same range of energy levels depicted in Figure 12.

Figure 14 is a chart illustrating the approximate shape of the combined cumulative probability that a circuit
25 will be cut without otherwise damaging the circuit over the same range of energy levels charted in Figures 12 and 13.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

A cut-link shaped in the form of a square pad is illustrated in Figure 3. The cut-link pad 20, is bonded to
30 a pair of lines 21 and 22, each positioned on the substrate of a chip or circuit board within a single plane. The pad and the lines are all electrically conductive, whereas that part of the substrate that contacts the metal is dielectric. Although this embodiment could just as fairly

microns. Accordingly, a pad designed to have a preferable length and width of two to three microns can absorb the bulk of the energy transmitted by the laser while remaining entirely within the beam spot.

5 Transfer of heat away from the cut-link is minimized by creating a comparatively-lower thermal resistance per unit length within the pad than without. Because the top layer of the substrate and any passivative coating are insulators, the primary mode through which heat is
10 transferred from the pad is through the connected lines. Accordingly, the direction of heat transfer out of the pad can be approximated as being along axis A-A', shown in Figure 3. Along axis A-A', thermal resistance is a function of the heat transfer coefficient of the conducting
15 material and the cross-sectional area of the conducting material measured in the plane normal to the axis. The pad and the lines are preferably comprised of a material with high thermal conductivity and high thermal expansion, such as aluminum and copper. In such a case, where the
20 composition of the pad is identical to the composition of each of the lines, a differential in thermal resistance is due primarily to a difference in cross-sectional area. The dimensions of the cross-section normal to the A-A' axis are illustrated in Figure 4. As shown, the cross-section of
25 the line (the product of w and h) is much smaller than the cross-section of the pad (the product of w' and h'). Accordingly, the thermal resistance along the A-A' axis will be much greater in each of the lines than in the pad. This differential reduces the loss of heat into and through
30 the line and thereby allows the temperature of the pad to quickly rise.

Moreover, the difference in thermal resistance produces a sharp temperature differential between the pad and the lines to create stress at the interface which
35 promotes a clean severance at the interface between the pad

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and the line. The difference in thermal resistance also creates a boundary limiting the area within which fracture will occur. I.e., fracture will not initiate from a comparatively cool region beyond the area where heat is concentrated. The differential on each side of the pad thereby ensures that fracture will commence from the pad, rather than from a line, providing greater cutting accuracy and minimizing damage to the surrounding circuitry.

Means other than increasing the width of the pad exist for creating a differential in thermal resistance at the interface of the pad and the line. For example, in one embodiment, the pad may be fabricated from a material having greater thermal conductivity than the material from which the lines are comprised. In another alternative embodiment, the pad may be both wider than the lines and comprised of a material having greater thermal conductivity than the lines.

In addition to improving the absorption and retention of thermal energy from the laser, creating a roughly square-shaped pad reduces the likelihood of producing a short circumventing the cut. As noted, the metal from the cut site escapes through fractures in the passivation layer. After or during a cut, the circuit will be shorted if metal migrates through the fractures to provide a continuous link from one line to the other. Because a comparatively large void is left after the ablation of a wide, square cut-link, the passage created by a fracture and the accompanying flow of metal linking the two lines must cover a greater distance to circumscribe the void and create a short. Further, cracks generated in the horizontal plane on which the circuit lies will typically emanate from the corners where stress is concentrated. As is shown in Figure 5, cracks 32a and 32b emanating from the edges 36 of a square-shaped pad 20 will typically be directed outward at an angle of 135° from the sides of the

pad 20 mitigating the likelihood that cracks from opposite sides of the pad will cross to create a passage for forming a short.

Designing the cut-link pad to approximate the size and shape of the laser beam spot also provides an additional benefit. Less energy misses the cut-link pad resulting in less energy being absorbed into the surrounding dielectric material which reduces the likelihood that this surrounding material will be damaged by thermal stresses.

Both the lines and the cut-links 20 in a circuit are coated with a passivation layer 30 to protect the circuit from oxidation as a result of exposure to air. For the cut-link 20 to be ablated, fractures 32 must be created within the passivation layer 30, which allow the section of passivation layer 30 covering the cut-link 20 to be blasted away from the chip, thereby exposing the cut-link 20 to air and allowing it to vaporize. Preferably, a hard, brittle material, such as silicon nitride is used as the passivation layer 30 because increasing hardness and brittleness is correlated with increasing susceptibility to fracture. When a laser pulse is incident on the cut-link pad 20, the cut-link pad 20 is heated and expands. The passivation layer 30 can not be heated as quickly as the metal lines because the passivation layer 30 can not absorb energy from the laser beam directly and can not conduct heat from the metal quickly. As a result, stress develops within the passivation layer 30 due to the difference in temperature between the metal 20 and the passivative coating 30 as well as the mismatch of the thermal expansion coefficients of the two materials. As the metal 20 expands with increasing temperature, greater tensile stress is placed on the passivative coating 30, which is why choosing a metal having a high thermal expansion coefficient is important. When the stress is sufficiently great, the passivative coating 30 is blasted from the area above the

cut-link 20, and the cut-link 20 vaporizes into the open space above it.

Typically, the substrate 34 of a chip includes a silicon wafer base upon which a dielectric material, such as a silicon oxide, is layered. The circuit is then imprinted onto the dielectric material. Because silicon nitride is more brittle than silicon oxide, fracture initiation is biased toward the silicon nitride. By promoting fracture through the passivation layer 30, rather than through the substrate 34, the metal is more likely to be completely ablated from the chip, and the likelihood of forming a short through the substrate is reduced. Though not as brittle as silicon nitride, silicon oxide is also sufficiently brittle to be used as the passivation layer 30.

Increasing the width of the cut-link also improves the fracture mechanics during ablation. The fracture initiates and grows as a result of thermal stress at the interface of the cut-link and the surrounding material. The thermal stress, in turn, is a function of the energy density at the surface of the pad. The lines of maximum stress, from which fractures typically propagate, are along the edge 36 of the pad 20 forming the perimeter of the surface 38 facing the passivation layer 30. The energy density along the maximum stress lines 36 is governed by the ratio of the energy absorbed to the length of the perimeter.

Making the approximating assumption that the energy density of the laser beam is uniform, the energy absorbed by a square surface 38 will be the product of k and S , where k is a constant and S represents the area of surface 38. The energy density, E_p , along the perimeter, P , of the surface 38 can be expressed by the function:

$$E_p = k * S / P$$

As the energy density increases, the stresses increase and the cracks grow. Energy density increases as a result of increasing the surface dimensions of the pad. As the dimensions increase, the area of the square, S ($S = l * w$),
5 increases as a square function while the length of the perimeter, P [$P = 2 * (l + w)$], increases linearly. Accordingly, S will increase at a quadratic rate while P increases at a linear rate. Because the numerator of the energy-density function increases with size at a rate
10 faster than the denominator, a fracture driven by a large, square-shaped cut-link will propagate through the passivation layer with greater energy than a fracture driven by a small or narrow cut-link.

Of course, fracture will initiate from an edge of the
15 outer surface because stress is concentrated at the edges. Use of a wider cut-link promotes fracture 32a from an edge 36 of the upper surface of the cut-link rather than fracture 32b from the lower surface facing toward the silicon wafer. After the fracture 32a has propagated
20 through the passivation layer 30, this segment of the passivation layer 30 can be "blown off" by the escaping metal, as desired. In contrast, fracture 32b commencing from the lower side can damage interconnects existing on lower levels of a chip, and the metal flowing through a
25 fracture directed toward the silicon has no outlet and is therefore more likely to produce a short. Therefore, the likelihood of producing a clean severance of an interconnect is promoted by the wider cut-links because fracture is biased toward the passivation layer and away
30 from the silicon wafer.

Although a preferred shape of the cut-link pad is square, other relatively compact shapes approximating the size and shape of the laser beam spot may also be used. Figure 7 illustrates a hexagonally-shaped pad of this
35 invention. As before, the width, w , of the pad is

approximately equal to the length, l , of the pad. Although this hexagonal design is more compact and provides a better approximation of the laser beam shape 24, as compared to a square pad, the crack 46 must propagate across a longer
5 distance to cross the interface between the line 21 and the pad 20. As the energy density builds along the edges 42 and 44, the pad 20 is severed from the line 21 when cracks 46, which parallel the edges 42, 44, branch across the interface.

10 Although each of the single-plane embodiments thus far described includes lines having widths uniformly narrower than the width of the cut-link pad, the width of the lines need not be uniform to provide benefit. Figures 8 and 9
15 illustrate embodiments wherein the cut-link and the lines 21 and 22 possess equal widths over much of their lengths. The width of each line 21, 22 narrows only as it approaches and where it meets the pad 20. Because the juncture of the line 21, 22 and the pad 20 is narrow, thermal resistance
20 along the A-A' axis increases at the juncture relative to the resistance within the pad, as in the previous embodiments. However, the overall ability to restrict heat flow out of the pad 20 may be somewhat compromised if the width beyond the bottleneck 50 is enlarged, as shown,
25 because the resistance in the line 21 or 22 drops to the level within the pad 20 at points beyond the bottleneck 50. Accordingly, heat can be rapidly withdrawn once it passes through the bottleneck 50 creating a more precipitous temperature drop across this interface thereby fueling the
30 conduction of heat out of the pad 20.

30 Another advantage of the patterns illustrated in Figures 8 and 9 is that the fracture along the interface of the pad 20 and the line 21 or 22 is enhanced. As noted,
above, fractures across the interface will typically emanate along a line substantially parallel to the edge 36
35 of the pad 20. In the pattern shown in Figure 3, the edge

of the line meets the edge of the pad perpendicularly. Accordingly, the stress along the edge of the line is perpendicular to the direction in which the interfacial fracture will propagate and will provide little or no
5 impetus toward initiating or driving this fracture. On the other hand, the edge 51 of the line 21 in Figure 8 slopes toward the edge 36 of the pad 20. In proportion to the component of this slope which parallels the edge 36 of the pad 20, the stress along the edge 51 of the line 21 will
10 supplement the stress along the edge 36 of the pad 20 to initiate and drive the fracture across the interface between the pad 20 and the line 21.

In contrast to the embodiments thus described, wherein the pad and the lines all lie within the same plane of a
15 chip or circuit board, the invention may also be embodied in multi-layered chips. Such an embodiment is illustrated in Figures 10 and 11. As before, the orientation of the pad 20 is parallel to the plane of the chip. However, in place of the laterally-extending lines, the lines take the
20 form of vias 21a and 22a extending downward from the surface 52 of the pad 20 away from the laser and into the substrate. These vias 21a and 22a provide a conductive link between levels of the integrated circuit. Typically, the vias 21a and 22a have a smaller cross-section than the
25 lines of the single-level embodiments. Where half-micron technology is used in standard silicon processing, the via 21a or 22a preferably has a width of about a half micrometer across its cross-section. The vias 21a and 22a are conductively coupled to the pad 20, which forms a
30 conductive cap stretching across and conductively bonded to the upper end of each via 21a, 22a. At their ends opposite the pad 20, the vias 21a and 22a are conductively bonded to lines 53, 54 extending laterally in a layer beneath the pad 20. By removing the pad 20 through laser ablation, the
35 conductive link is broken.

When the laser strikes the pad 20, heat migrates downward away from surface. During the first few nanoseconds after the laser strikes, the temperature at the bottom 52 of the pad is much lower than the temperature at the top surface 38. As a result, less heat is dissipated through the vias 21a, 22a than if they were laterally connected, and the efficiency with which the cut is performed is thereby improved.

In either a single-layer or multi-layer embodiment of the electrical interconnect, the method for ablating the cut-link pad is substantially identical. First, a laser beam having an intensity on the order of 10 Joules per square centimeter is directed onto the site of the pad. When embodied in a chip, the pad is typically coated with a passivation layer. The beam must be able to pass through the passivation layer, which is preferably silicon nitride, and be absorbed by the metal of the cut-link pad. The wavelength of the laser beam is determined by what is transmittable through the passivation layer. Each material has an upper limit as to the size of the wavelength that it is capable of absorbing. For silicon nitride, that limit is about a half micrometer. Therefore, an infrared laser producing a beam with a wavelength of about one micrometer may be used to transmit energy through the silicon nitride layer to the underlying metallic cut-link pad where it is absorbed.

The laser generates a beam in the form of a pulse or a series of pulses. The duration of the pulse is determined by the thickness of the pad and the rate of thermal diffusion through the pad. With these variables in mind, the pulse should be of sufficient duration for the heat to diffuse through the entirety of the pad. For the embodiments thus far described, a pulse of 5 to 10 nanoseconds is generally sufficient to produce a clean severance without damage to the circuit.

Damage can occur when too much energy is directed at the cut-link site. Specifically, excessive energy is created by a pulse having excessive intensity or excessive duration. On one hand, the pulse and duration must be

5 sufficiently great to supply ample energy to initiate and drive the fracture severing the pad from the lines and expelling the overlying passivation layer. The remaining energy must be sufficient to vaporize the cut-link pad and produce a substantially vacant cavity at the former site of

10 the pad. If too much energy is provided, however, a crack 32b can propagate, as shown in Figure 5, from the lower corner of the pad 20 through the dielectric material and damage the underlying circuitry.

The relation between the amount of laser-supplied

15 energy and the probability of producing a clean severance of the circuit without damage is illustrated in the generalized cumulative probability functions charted in Figures 12-14. Figure 12 illustrates the approximate shape of a cumulative probability curve 56 measuring the

20 likelihood that a circuit will be severed at increasing energy levels. Figure 13 illustrates the approximate shape of a cumulative probability curve 58 measuring the likelihood that a circuit will be damaged across a range of increasing energy levels. By subtracting the probability

25 of damaging a circuit from the probability of severing a circuit (*i.e.*, by subtracting the values of the chart in Figure 13 from the values of the chart in Figure 12), the probability of clean severance, *i.e.*, severing a circuit without damaging it, is obtained as a function of energy.

30 A curve 60 approximating the plot of this probability function is charted in Figure 14. For optimal results, the intensity and duration of the pulse should be set at levels to produce the energy at which the probability of a clean severance most nearly approaches 1.0. The limit of $P = 1.0$

35 represents a certainty that the circuit will be severed

CLAIMS

1. An electrical interconnect comprising:
 - a substrate having an insulating surface;
 - a first electrically-conductive line on the
 - 5 insulating surface of the substrate;
 - a second electrically-conductive line on the
 - insulating surface of the substrate; and
 - an electrically-conductive cut-link pad on the
 - insulating surface of the substrate, the cut-link pad
 - 10 conductively bonded between the first conductive line
 - and the second conductive line, the cut-link pad also
 - having substantially less thermal resistance per unit
 - length than each of the first and second lines.
2. The interconnect of Claim 1, wherein the electrically-
15 conductive cut-link pad lies in the same plane as the
- first and second electrically-conductive lines.
3. The interconnect of Claim 1, wherein the electrically-
20 conductive cut-link pad has an inner surface facing
- the substrate and an opposing outer surface facing
- away from the substrate, the first and second
- electrically-conductive lines extending from the inner
- surface into the substrate.
4. The interconnect of Claim 1, wherein the electrically-
25 conductive cut-link pad has an inner surface facing
- the substrate, the first electrically-conductive line
- extending from the inner surface into the substrate,
- the second electrically-conductive line lying in the
- same plane as the cut-link pad.
5. The interconnect of Claim 1, wherein the width of the
30 cut-link pad is at least ten percent greater than the

13. The interconnect of Claim 12, wherein the passivative layer is harder than the substrate.
14. The interconnect of Claim 13, wherein the passivative layer is comprised of silicon nitride.
- 5 15. The interconnect of Claim 12, wherein the electrically-conductive cut-link pad lies in the same plane as the first and second electrically-conductive lines.
- 10 16. The interconnect of Claim 12, wherein the electrically-conductive cut-link pad has an inner surface facing the substrate and an opposing outer surface facing away from the substrate, the first and second electrically-conductive lines extending from the inner surface into the substrate.
- 15 17. The interconnect of Claim 12, wherein the width of the cut-link pad is at least fifty percent greater than the width of each of the first and second electrically-conductive lines.
- 20 18. The interconnect of Claim 17, wherein the substrate is planar and the width of the cut-link pad is within 20% of the length of the cut-link pad, the length being measured as the distance across the cut-link pad between the first and second lines.
- 25 19. The interconnect of Claim 12, wherein the cut-link pad is comprised of a material with greater thermal conductivity than the material comprising each of the first and second electrically-conductive lines.

20. A method for cutting a link between interconnected circuits comprising the following steps:
- directing a laser upon an electrically-conductive cut-link pad conductively bonded between a first electrically-conductive line and a second electrically-conductive line on a substrate, the cut-link pad having substantially less thermal resistance per unit length than each of the first and second lines; and
- maintaining the laser upon the cut-link pad until the laser infuses sufficient energy into the cut-link pad to break the conductive link across the cut-link pad between the pair of electrically-conductive lines.
21. The method of Claim 20, wherein the electrically-conductive cut-link pad lies in the same plane as the first and second electrically-conductive lines.
22. The method of Claim 20, wherein the electrically-conductive cut-link pad has an inner surface facing the substrate and an opposing outer surface facing away from the substrate, the first and second electrically-conductive lines extending from the inner surface into the substrate.
23. The method of Claim 22, wherein the laser beam extends across the entirety of the cut-link pad when the laser is directed upon the cut-link pad.
24. The method of Claim 20, wherein the electrically-conductive cut-link pad has an inner surface facing the substrate, the first electrically-conductive line extending from the inner surface into the substrate, the second electrically-conductive line lying in the same plane as the cut-link pad.

25. The method of Claim 20, wherein the width of the cut-link pad is at least ten percent greater than the width of each of the first and second electrically-conductive lines.
- 5 26. The method of Claim 20, wherein the width of the cut-link pad is at least twenty-five percent greater than the width of each of the first and second electrically-conductive lines.
- 10 27. The method of Claim 20, wherein the width of the cut-link pad is at least fifty percent greater than the width of each of the first and second electrically-conductive lines.
- 15 28. The method of Claim 27, wherein the cut-link pad is comprised of a composition substantially identical to the composition of the first and second electrically-conductive lines.
- 20 29. The method of Claim 28, wherein the substrate is planar and the width of the cut-link pad is within 20% of the length of the cut-link pad.
30. The method of Claim 29, wherein the laser beam extends across the entirety of the cut-link pad when the laser is directed upon the cut-link pad.
- 25 31. The method of Claim 20, wherein the material comprising the cut-link pad has greater thermal conductivity than the material comprising each of the first and second electrically-conductive lines.
32. The method of Claim 20, wherein the substrate includes a silicon oxide.

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33. The method of Claim 20, further comprising a passivative layer covering the cut-link pad.
34. The method of Claim 33, wherein the passivative layer is harder than the substrate.
- 5 35. The method of Claim 34, wherein the passivative layer is comprised of silicon nitride.
36. The method of Claim 33, wherein the electrically-conductive cut-link pad lies in the same plane as the first and second electrically-conductive lines.
- 10 37. The method of Claim 33, wherein the electrically-conductive cut-link pad has an inner surface facing the substrate and an opposing outer surface facing away from the substrate, the first and second electrically-conductive lines extending from the inner
15 surface into the substrate.
38. The method of Claim 37, wherein the laser beam extends across the entirety of the cut-link pad when the laser is directed upon the cut-link pad.
39. The method of Claim 33, wherein the width of the cut-
20 link pad is at least fifty percent greater than the width of each of the first and second electrically-conductive lines.
40. The method of Claim 39, wherein the substrate is planar and the width of the cut-link pad is within 20%
25 of the length of the cut-link pad, the length being measured as the distance across the cut-link pad between the first and second lines.

LASER-INDUCED CUTTING OF METAL INTERCONNECT

Abstract of the Disclosure

An electrical interconnect includes a substrate having an insulating surface upon which is placed an electrically-
5 conductive cut-link pad and a pair of electrically-
conductive lines. The lines are bonded to the cut-link pad and are substantially more resistant to heat flow per unit length than is the cut-link pad. In a preferred
10 embodiment, the thermal resistance per unit length of the cut-link pad is lowered by designing the pad such that its width is greater than the width of either of the lines. A method for cutting a circuit includes directing a laser upon the cut-link pad of an interconnect, as described
15 above. The laser is maintained upon the pad until the cut-link pad is ablated, severing the circuit.

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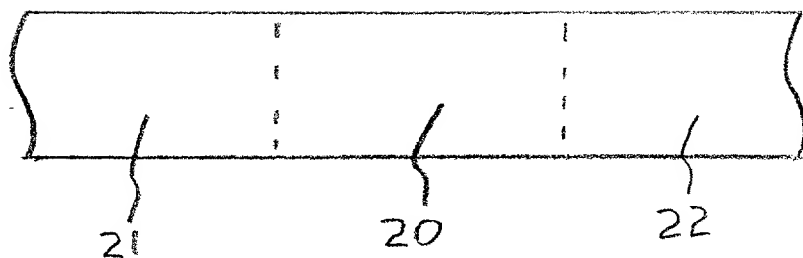


Fig. 1
Prior Art

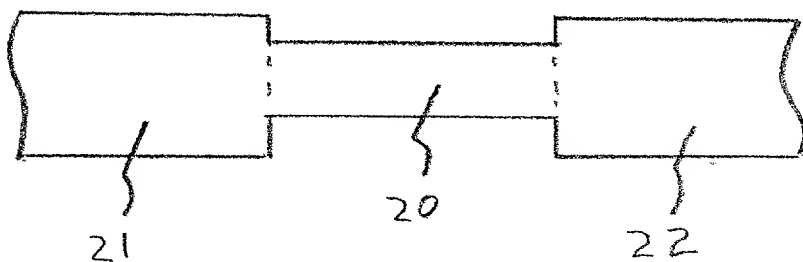


Fig. 2
Prior Art

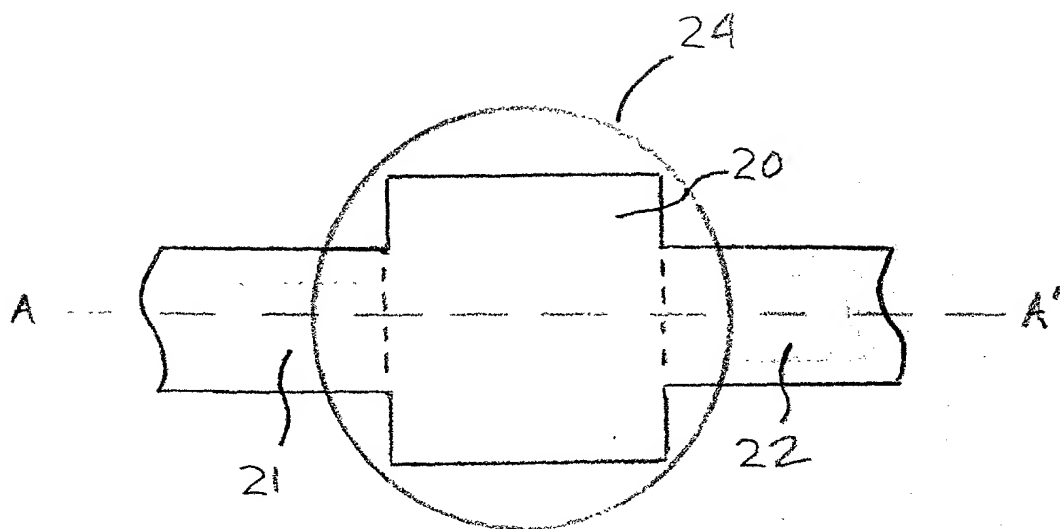


Fig. 3

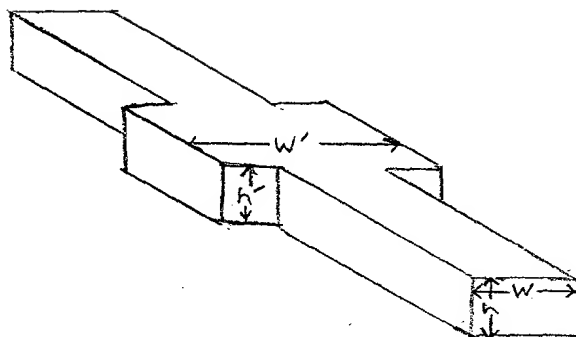


Fig. 4

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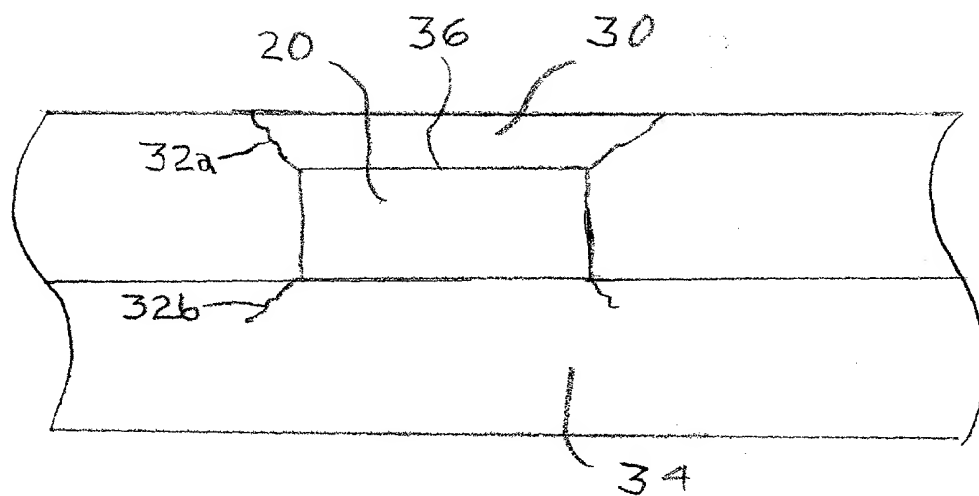


Fig. 5

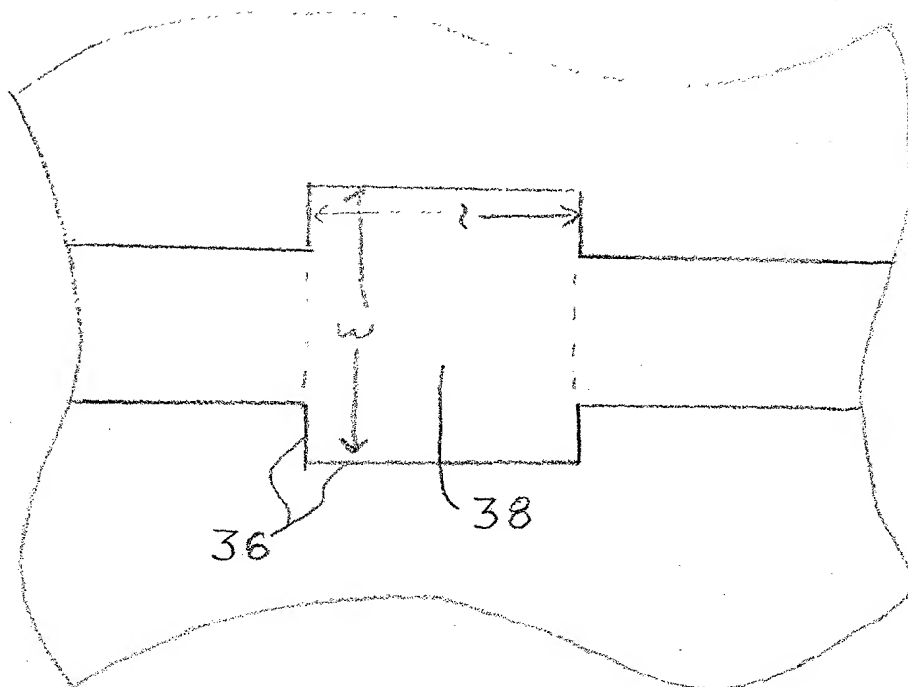


Fig 6

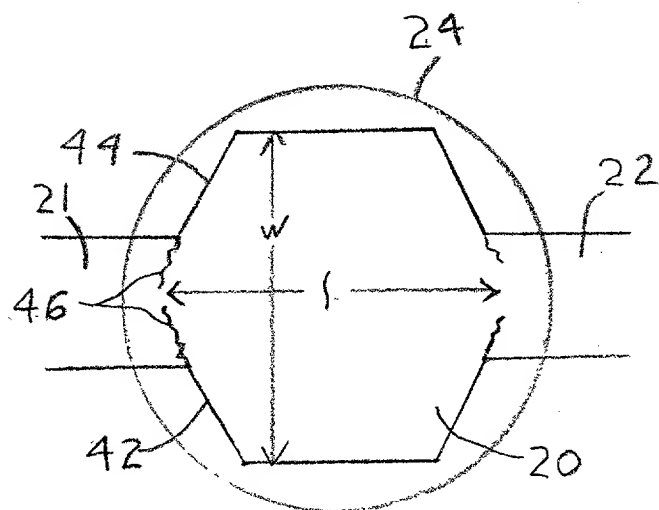


Fig. 7

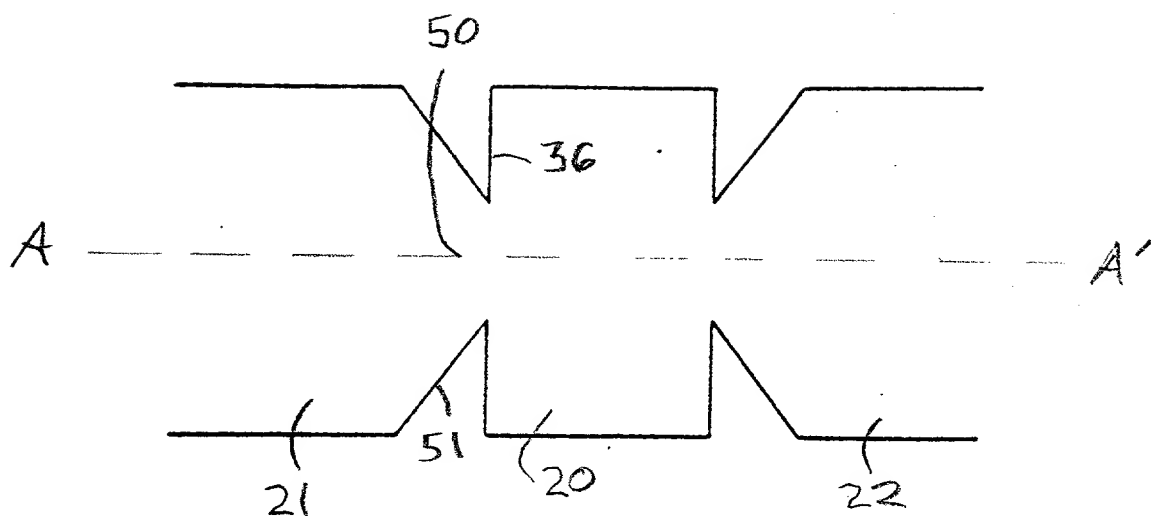


Fig. 8

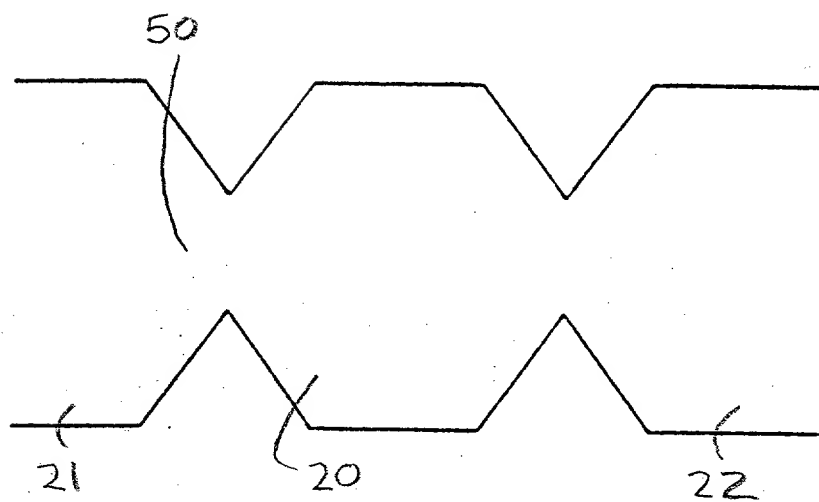


Fig. 9

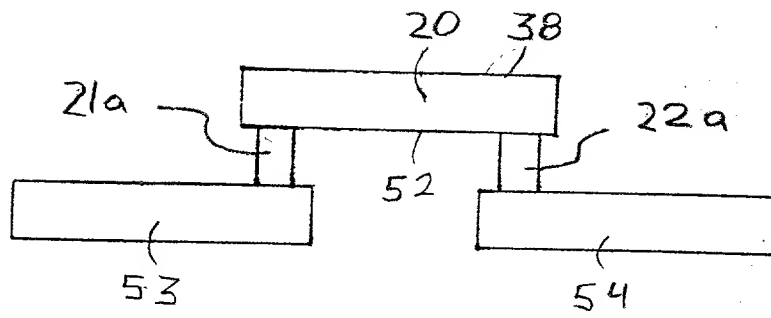


Fig. 10

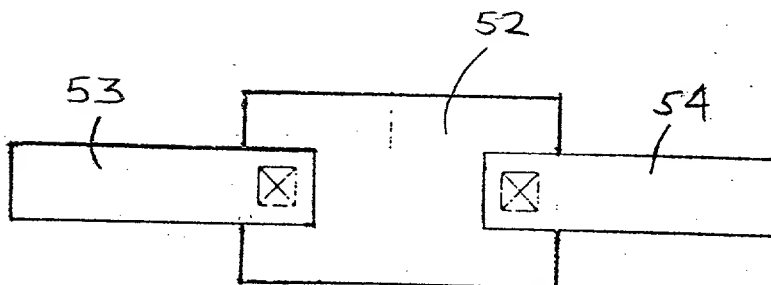


Fig. 11

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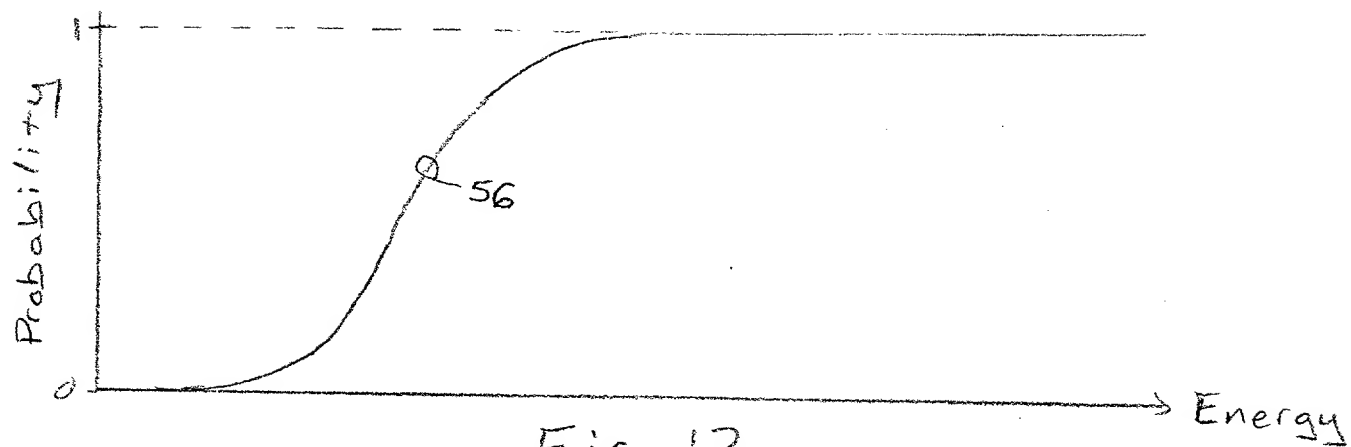


Fig. 12

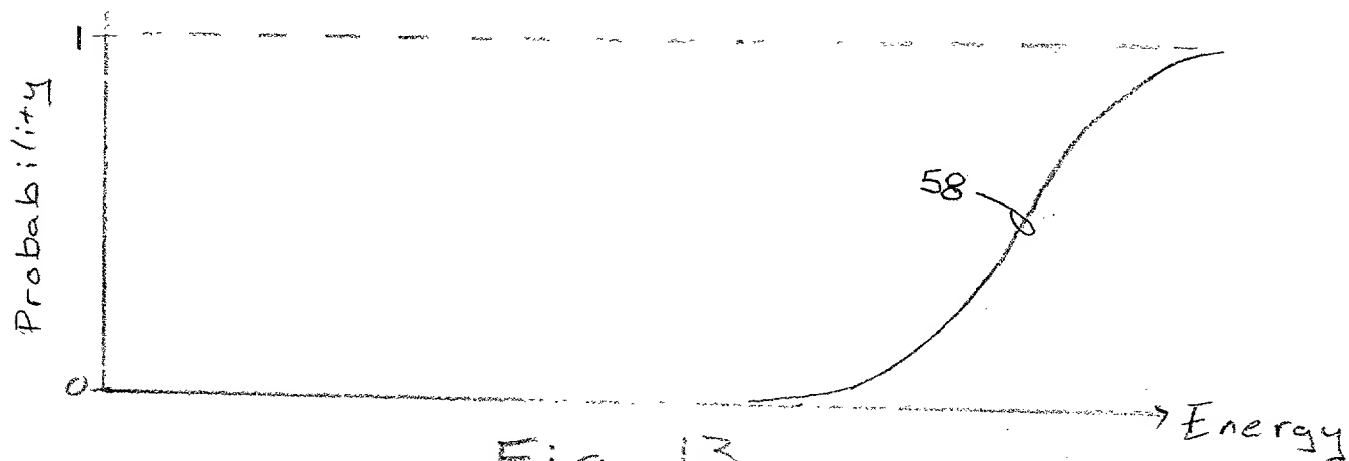


Fig. 13

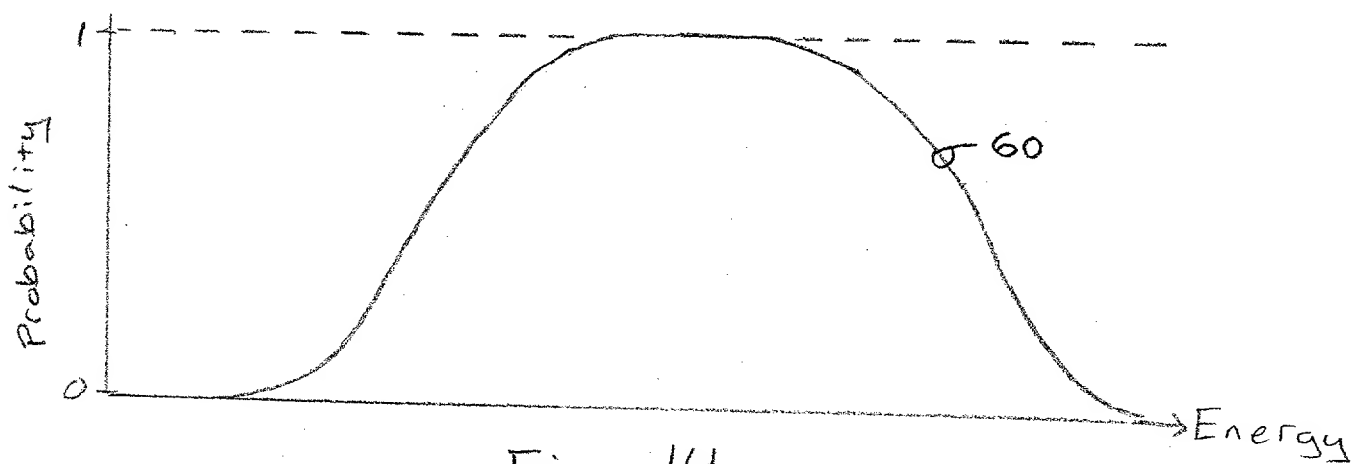


Fig. 14

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Declaration for Patent Application

As a named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name;

I believe I am the original, first and sole inventor (if only one name is listed) or an original, first and joint inventor (if plural names are listed in the signatory page(s) commencing at page 3 hereof) of the subject matter which is claimed and for which a patent is sought on the invention entitled

LASER-INDUCED CUTTING OF METAL INTERCONNECT

the specification of which (check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application

Number or PCT International Application Serial No. _____

and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known by me to be material to patentability as defined in 37 C.F.R. §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

<u>Prior Foreign Application(s)</u>			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year filed)	<input type="checkbox"/>
_____ (Number)	_____ (Country)	_____ (Day/Month/Year filed)	<input type="checkbox"/>
_____ (Number)	_____ (Country)	_____ (Day/Month/Year filed)	<input type="checkbox"/>

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

_____ (Application Number)	_____ (Filing Date)
_____ (Application Number)	_____ (Filing Date)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information known by me to

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be material to patentability as defined in 37 C.F.R. §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.) (Filing date) (Status, patented, pending, abandoned)

(Application Serial No.) (Filing date) (Status, patented, pending, abandoned)

As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

I also hereby grant additional Powers of Attorney to the following attorney(s) and/or agent(s) to file and prosecute an international application under the Patent Cooperation Treaty based upon the above-identified application, including a power to meet all designated office requirements for designated states:

David E. Brook	Reg. No. 22,592	Thomas O. Hoover	Reg. No. 32,470
James M. Smith	Reg. No. 28,043	Alice O. Carroll	Reg. No. 33,542
Leo R. Reynolds	Reg. No. 20,884	N. Scott Pierce	Reg. No. 34,900
Patricia Granahan	Reg. No. 32,227	Richard A. Wise	Reg. No. 18,041
Mary Lou Wakimura	Reg. No. 31,804		

all of Hamilton, Brook, Smith and Reynolds, P.C., Two Militia Drive, Lexington, Massachusetts 02173;

and

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Direct telephone calls to: James M. Smith

(617) 861-6240

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full name of sole

or first inventor Joseph B. Bernstein

Inventor's

Signature

Date

3/21/97

Residence

7814 Ivy Mount Terrace

Potomac, Maryland 20854

Citizenship

USA

Post Office Address

same as above

Full name of second joint

inventor, if any Zhihui Duan

Second Inventor's

Signature _____ Date _____

Residence 1566 West 54th Street

Erie, Pennsylvania 16509

Citizenship China

Post Office Address same as above

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Declaration for Patent Application

As a named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name;

I believe I am the original, first and sole inventor (if only one name is listed) or an original, first and joint inventor (if plural names are listed in the signatory page(s) commencing at page 3 hereof) of the subject matter which is claimed and for which a patent is sought on the invention entitled

LASER-INDUCED CUTTING OF METAL INTERCONNECT

the specification of which (check one)

☒ is attached hereto.

☐ was filed on _____ as United States Application

Number or PCT International Application Serial No. _____

and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is known by me to be material to patentability as defined in 37 C.F.R. §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

<u>Prior Foreign Application(s)</u>			Priority Not Claimed
_____ (Number)	_____ (Country)	_____ (Day/Month/Year filed)	[]
_____ (Number)	_____ (Country)	_____ (Day/Month/Year filed)	[]
_____ (Number)	_____ (Country)	_____ (Day/Month/Year filed)	[]

I hereby claim the benefit under 35 U.S.C. §119(e) of any United States provisional application(s) listed below.

_____ (Application Number)	_____ (Filing Date)
_____ (Application Number)	_____ (Filing Date)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information known by me to

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be material to patentability as defined in 37 C.F.R. §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing date)	(Status, patented, pending, abandoned)
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(Application Serial No.)	(Filing date)	(Status, patented, pending, abandoned)
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As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

I also hereby grant additional Powers of Attorney to the following attorney(s) and/or agent(s) to file and prosecute an international application under the Patent Cooperation Treaty based upon the above-identified application, including a power to meet all designated office requirements for designated states:

David E. Brook	Reg. No. 22,592	Thomas O. Hoover	Reg. No. 32,470
James M. Smith	Reg. No. 28,043	Alice O. Carroll	Reg. No. 33,542
Leo R. Reynolds	Reg. No. 20,884	N. Scott Pierce	Reg. No. 34,900
Patricia Granahan	Reg. No. 32,227	Richard A. Wise	Reg. No. 18,041
Mary Lou Wakimura	Reg. No. 31,804		

all of Hamilton, Brook, Smith and Reynolds, P.C., Two Militia Drive, Lexington, Massachusetts 02173;

and

Send correspondence to: James M. Smith, Esq.

Hamilton, Brook, Smith & Reynolds, P.C.
Two Militia Dr., Lexington, MA 02173

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